MACHAKOS UNIVERSITY

University Examinations for 2021/2022 Academic Year

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

THIRD YEAR SECOND SEMESTER EXAMINATIONS FOR

BACHELOR OF SCIENCE (MECHANICAL ENGINEERING)

EMM 300: ENGINEERING ELECTRONICS

DATE: **TIME: 2 Hours**

INSTRUCTIONS

Answer Question One And Any Other Two Questions

QUESTION ONE (COMPULSORY) (30 MARKS)

a) A diode whose internal resistance is 20Ω is to supply power to a 1000 Ω load from a 110 V (rms) source of supply. Calculate:
   i. The peak load current;
   ii. The DC load current;
   iii. AC Load Current;
   iv. The DC diode voltage;

(8 marks)

b) Determine the dc bias voltage V_{CE} and the current I_C for the CE BJT voltage divider circuit configuration.
Assume V_{CC} = 22 V, R_1= 39 kΩ, R_2 = 3.9 kΩ, R_C = 10 kΩ, R_E = 1.5 kΩ and β = 100. **(**8 marks)

c) Simplify the following Boolean expressions using Boolean algebra and/or De Morgan's theorem.

   i.

$$\overline{(A+\overline{B})(\overline{A\overline{C}\overline{D}})}$$

ii.

$$(\overline{\overline{A}\oplus\overline{BC}})(\overline{A+B+\overline{C}})$$

(6 marks)

d) Assuming that all numbers are 8 bits wide, complete the missing entries, which are not shaded, in the following table. (No marks will be awarded for this question unless you show how the solution is derived.)

Hexadecimal	Octal	Signed binary	Signed decimal
?		?	-105
?	275		?

(8 marks)

QUESTION TWO (20 MARKS)

a) Describe the following regions of operation of a common emitter transistor amplifier:
(i) Cut-off;
(ii) Active;
(iii) Saturation.

(6 marks)

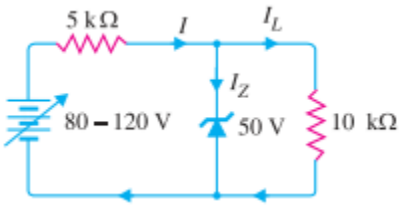
b) Explain the term thermal run-away with respect to BJT circuits.

(2 marks)

c) A silicon transistor using the voltage divider bias method has the following parameters: R_1 = 33 KΩ, R_2 = 15 KΩ, R_C = 1KΩ, R_E = 680 Ω and V_{CC} = 9 V. Determine the operating point of this transistor circuit.

(5 marks)

d) For the circuit shown in FigQ2 (d), find the maximum and minimum values of zener diode current.

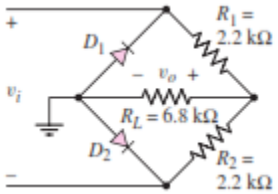


FigQ2 (d)

(4 marks)

e) i. Sketch v_o versus time for the circuit in FigQ2 (e). The input is a sine wave given by $v_i = 10 \sin \omega t$ V. Assume $V_\gamma = 0$.

ii. Determine the rms value of the output voltage.

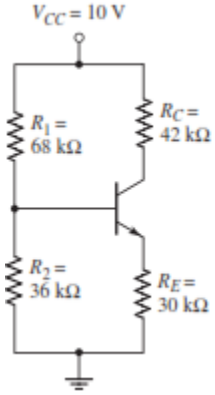


(3 marks)

QUESTION THREE (20 MARKS)

a) i. Determine the *Q*-point values for the circuit in FigQ3 (a). Assume β = 50

ii. Repeat part (i) if all resistor values are reduced by a factor of 3.



FigQ3 (a)

(10 marks)

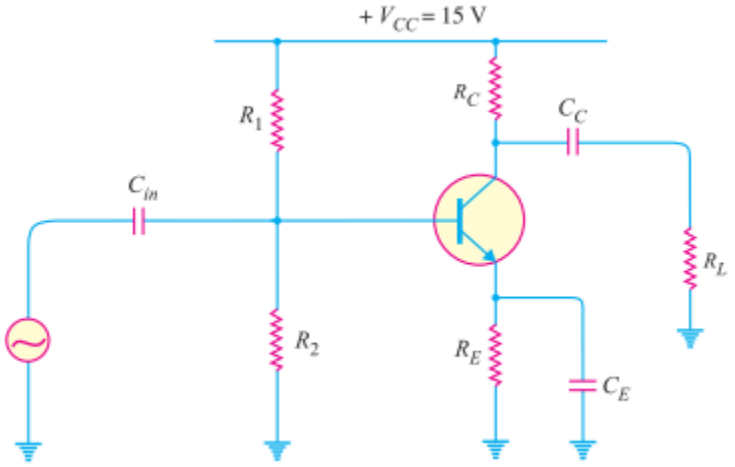
b) For the transistor amplifier shown in FigQ3 (b) R_1 = 10 kΩ, R_2 = 5 kΩ, $R_C = R_L$ = 1 kΩ, and R_E = 2 kΩ

i. Draw d.c. load line;

ii. Determine the operating point;

iii. Draw a.c. load line.

Assume V_{BE} = 0.7 V.



FigQ3 (b)

(10 marks)

QUESTION FOUR (20 MARKS)

a) Simplify the following Boolean expressions using Boolean algebra and/or De Morgan's theorem.

i. $\overline{A}\overline{B}C + \overline{B}\overline{C} + AB\overline{C}$

ii $\overline{\overline{(A \oplus B)}(\overline{A} + B + BC)}$

(8 marks)

b) Simplify the following Boolean equation, in product-of-sums form, using a Karnaugh map.

$f = A\overline{B} + \overline{A}BC + AB\overline{C}$

(4 marks)

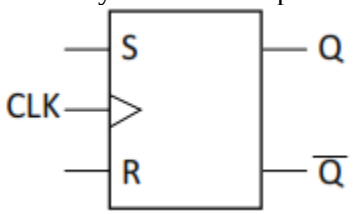
c) Assuming that all numbers are 8 bits wide, complete the missing entries, which are not shaded, in the following table. (No marks will be awarded for this question unless you show how the solution is derived.)

Hexadecimal	Octal	Unsigned decimal	Signed decimal	BCD
C5		?	?	
?	25			?

(8 marks)

QUESTION FIVE (20 MARKS)

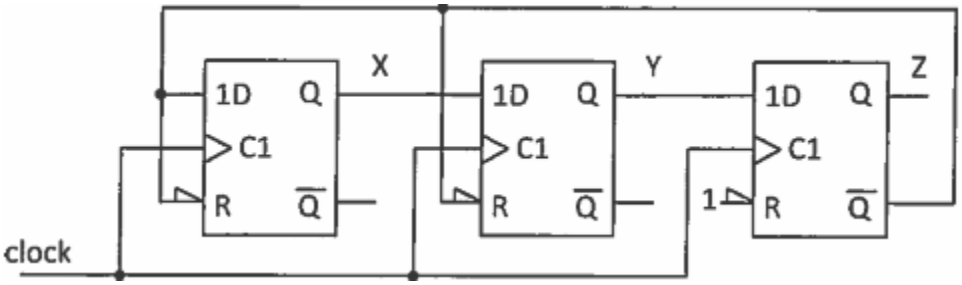
a) FigQ5 (a) shows a clocked SR-type flip-flop. Implement this flip-flop using a D-type flip-flop. You may assume that any disallowed input combinations do not occur.



FigQ5 (a)

(8 marks)

b) For the circuit shown in FigQ5 (b), complete the timing waveforms for signals X, Y, and Z for 6 clock cycles. You may assume that initially, the values of X, Y and Z are zero.



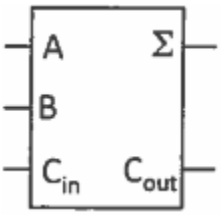
FigQ5 (b)

(6 marks)

c) A full-adder is shown in FigQ5 (c). For inputs A, B, and C_{in}, and outputs $\sum$ and C_{out}:

i. Draw the truth table for the circuit;

ii. Hence, derive Boolean expression for $\sum$ and C_{out}.



FigQ5 (c)

(6 marks)